Lab for High Performance Computing
Department of Computer Science and Automation
Convenor : Prof. R. Govindarajan

Cache Placement & Replacement Policies
- Improving cache hit rates using next-use distance estimates
- Adaptive cache placement to reduce conflict misses
- Two-level mapping based placement
- Emulating the optimal placement policy with a shepherd cache

Network Processor Architecture
- Design space exploration of network processors
- Packet reordering in network processors
- Petri net models to evaluate packet buffering in network processors
- Distributed packet buffering and dynamic buffering schemes
- Improving performance of table lookup operations
- Framework for application design space exploration

Prefetching
- Estimation of prefetch history effectiveness using entropy
- Identifying and eliminating misses that cause pipeline stalls

Memory Hierarchy

General Purpose

Micro-architecture

Network Processors

Application Specific

Embedded Systems

Memory Arch. Exploration
- Evolutionary approach for memory architecture exploration
- Integration of architecture and data layout exploration
- Pareto optimal design points for power, performance and cost
- Hybrid memory architectures involving cache and scratchpads

Power Performance Efficient Architectures
- Segmented low power issue queues
- Scalable energy efficient store queues
- Heterogeneous width register files for superscalar architectures

ARCHITECTURE

Students : Graduated (Current)

ME/MTech	:	13 (0)
MSc(Engg)	:	16 (2)
PhD	:	3 (5)

Programmability
Performance
Power Efficiency

Software Transactional Memory
- Compiler transformations to improve cache performance
- Compiler transformations to reduce number of conflicts

Compiler Optimizations
- Code size aware instruction scheduling
- Energy aware compilation techniques, exploiting DVFS
- Energy aware instruction scheduling and S/W pipelining

HPC

COMPILERS

Distributed Shared Memory
- Compiler and software assisted distributed shared memory (DSM)

Compiler Analysis
- Scalable context-sensitive points-to analysis through randomization
- Points-to analysis as a system of linear equations
- Comprehensive path-sensitive data flow analysis

Clusters
- Cluster based web servers
- Cache performance for web server architectures
- Exploiting communication processors for improving application performance

Compilers for Heterogeneous Architectures
- Synergistic use of general purpose and accelerator architectures
- Framework for automatic compilation of Matlab programs for heterogeneous architectures – MEGHA
- Compilation of X10 for heterogeneous architectures
- Coarse grained S/W pipelined execution of stream programs

Compiler Optimizations
- Instruction scheduling, register allocation
- Software pipelining (SWP)
  - Nested loop SWP
  - Energy aware SWP
  - Register sensitive SWP
  - Enhanced coscheduling
- Resource usage models for instruction scheduling and s/w pipelining
- Vectorizing compilers for MMX

Research Funding
AMD, DST, IBM, Intel, Microsoft, NVIDIA

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